PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jeffrey S. Mailloux et al. Examiner: Hong Chong Kim

Serial No.: 08/650,719 Group Art Unit: 2185

Filed: May 20, 1996 Docket: 303.623US1

For: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

AMENDED APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

This Amended Appeal Brief is presented in response to the Notification of Non-Compliant Appeal Brief mailed on July 12, 2007.

The original Appeal Brief was presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on March 8, 2007, and in response to the Final Rejection of claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 of the above-identified Application, as set forth in the Final Office Action mailed on February 20, 2007.

The entire appeal brief, amended to include the sections identified as being in need of correction in the Notification of Non-Compliant Appeal Brief, is submitted herewith. The requisite fee of $500.00 set forth in 37 C.F.R. § 41.20(b)(2) was previously paid with the original Appeal Brief submission. The Appellant respectfully requests review and reversal of the rejections of the pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC.

2. RELATED APPEALS AND INTERFERENCES

A first, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowance indicating allowance of all claims was subsequently mailed to the Appellant, and the application has now issued as U.S. Pat. No. 6,615,325. This matter never appeared before the Board.

A second, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2). The Board issued a decision in this matter, allowing all claims (Appeal 2004-0414, attached hereto), and the application has now issued as U.S. Pat. No. 7,103,742. This matter is no longer before the Board.

A third, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). The Board issued a decision in this matter, allowing all claims (Appeal 2004-1705, attached hereto). The application has not yet issued, and is no longer before the Board.

A fourth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,562 (Atty. Ref. No. 303.623US3). The Board issued a decision in this matter, allowing all claims except claim number 61 (Appeal 2005-1725, attached hereto), and the application has now issued as U.S. Pat. No. 7,124,256. This matter is no longer before the Board.

A fifth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,563 (Atty. Ref. No. 303.623US4). Since this fifth appeal was only recently filed (on January 25, 2007), the matter is still pending before the Board.

An appeal was filed with respect to the instant matter (U.S. Patent Application Serial Number 08/650,719; Atty. Ref. No. 303.623US1) on January 16, 2004. Prosecution was reopened by the Examiner, and a supplemental appeal brief was filed August 11, 2004. Prosecution was again reopened by the Examiner, and after receiving a final rejection, the Appellant has filed this Appeal in response.

There are no other appeals, interferences, or judicial proceedings known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present Application was filed on May 20, 1996 with claims 1-58. Claims 11-32, 36-45, and 51-58 were canceled in response to a restriction requirement, the response being filed on November 3, 1997. Claims 10 and 47 were canceled, and claims 3-9, 33-35, 46, and 48-50 were amended in a response filed on December 7, 1998. Claims 1, 33, and 50 were amended in a response filed on April 27, 1999. Claim 50 was amended in a response filed on September 2, 1999. At this point, claims 1-9, 33-35, 46, and 48-50 were pending.

Claim 50 was amended, and new claims 59-64 were added in a response filed on September 30, 1999. Claims 46 and 61 were amended in a response filed on March 19, 2000. Claim 62 was canceled in response to a restriction requirement, the response being filed on November 7, 2000. Claim 61 was amended in a response filed on May 2, 2001. Claim 7 was amended in a response filed on May 31, 2002, and again in a response filed on September 16, 2002. Finally, claim 61 was amended in a response filed December 22, 2006. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 stand twice rejected and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made in response to, or subsequent to the Final Office Action mailed February 20, 2007.

5. SUMMARY OF CLAIMED SUBJECT MATTER

This summary is presented in compliance with the requirements of Title 37 C.F.R. § 41.37(c)(1)(v), mandating a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal ...". Nothing contained in this summary is intended to change the specific language of the claims described, nor is the language of this summary to be construed so as to limit the scope of the claims in any way.

[Application, independent claim 1; FIGs. 9-12; pg. 25, line 7 - pg. 33, line 21]

Some embodiments of the invention are related to an asynchronously-accessible storage device 100 comprising mode circuitry 138 configured to select between a burst mode and a pipelined mode, and circuitry 122 operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry 138 and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device 100 in either mode.

[Application, independent claim 33; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21]

Some embodiments of the invention are related to a method for accessing a storage device 100, comprising receiving 154 a first address to the storage device 100, selecting 159 between an asynchronously-accessible burst mode 160 and an asynchronously-accessible pipelined mode 158 of operation of the storage device 100, selecting 150, 161 between outputting information from the storage device 100 and inputting information to the storage device 100, obtaining 151, 155, 162, 168 a second address to the storage device, and asynchronously accessing 152, 156, 163, 169 a storage element of the storage device in the selected mode of operation using the first address and the second address.

[Application, independent claim 46; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21]

Some embodiments of the invention are related to method for accessing several different locations in an asynchronously-accessible memory device 100, comprising selecting 159 a pipelined mode 158 of operation, providing 151, 155 a new external address for every access

152, 156 associated with asynchronously accessing the asynchronously-accessible memory device 100 while in the pipelined mode 158 of operation, switching 159 modes to a burst mode 160 of operation, providing 162, 168 an initial external address associated with asynchronously accessing the asynchronously-accessible memory device 100 in the burst mode 160 of operation, and generating 164, 170 at least one subsequent internal address patterned after the initial external address 162, 168 while in the burst mode of operation.

[Application, independent claim 50; FIGs. 9-12, and 20; pg. 25, line 7 - pg. 33, line 21, and pg. 40, lines 16-19]

Some embodiments of the invention are related to a system 255 comprising a microprocessor 251; a memory 100 coupled to the microprocessor 251, the memory 100 selectively operable either in a burst mode or a pipelined mode, wherein the memory 100 is an asynchronous dynamic random access memory; and a system clock 253 coupled to the microprocessor 251.

[Application, independent claim 59; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21]

Some embodiments of the invention are related to a method for accessing a storage device 100, comprising receiving 154 a first address to the storage device 100, receiving a burst/pipeline signal 110 to select 159 between an asynchronously-accessible burst mode 160 and an asynchronously-accessible pipelined mode 158 of operation of the storage device 100 in response to the burst/pipeline signal 110, obtaining 151, 155, 162, 168 a second address to the storage device 100, and accessing 152, 156, 163, 169 a storage element of the storage device 100 in the selected mode of operation using the first address and the second address.

[Application, independent claim 60; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21]

Some embodiments of the invention are related to a method for accessing a storage device 100, comprising receiving 154 a first address to the storage device 100, receiving a burst/pipeline signal 110 to select 150, 161 between outputting information from the storage device 100 and inputting information to the storage device 100, selecting 159 between an

asynchronously-accessible burst mode 160 and an asynchronously-accessible pipelined mode 158 of operation of the storage device 100 in response to the burst/pipeline signal 110, obtaining 151, 155, 162, 168 a second address to the storage device 100, and asynchronously accessing 152, 156, 163, 169 a storage element of the storage device 100 in the selected mode of operation using the first address and the second address.

[Application, independent claim 61; FIGs. 9, 12; pg. 30, line 24 - pg. 33, line 21]

Some embodiments of the invention are related to a method for accessing several different locations in an asynchronously-accessible memory device 100, comprising selecting 159 a pipeline mode 158 of operation, providing 151, 155 an initial external address associated with asynchronously accessing the asynchronously-accessible memory device 100 in the pipeline mode of operation, switching 159 modes to a burst mode 160 of operation, while in the burst mode 160 of operation, generating 164, 170 at least one subsequent internal address patterned after the initial external address 151, 155 provided while in the pipelined mode 158 of operation; and providing 162, 168 a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode 160 of operation.

[Application, independent claim 63; FIGs. 9-12; pg. 25, line 7 - pg. 33, line 21]

Some embodiments of the invention are related to a storage device 100, comprising an array 111 of memory cells, mode circuitry 138 for receiving a burst/pipeline signal 110, and operation circuitry 122 operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal 110, the operation circuitry 122 switchable between burst and pipeline modes of operation.

[Application, independent claim 64; FIGs. 9-12; pg. 25, line 7 - pg. 33, line 21]

Some embodiments of the invention are related to a memory circuit 100 comprising an array 111 of memory cells, burst/pipeline selection circuitry 138 for determining a burst or a pipeline mode of operation of the memory circuit 100, and mode circuitry 122 capable of

operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.

This summary does not provide an exhaustive or exclusive view of the subject matter of the Application, and the Appellant refers the reader to the appended claims and their legal equivalents for a complete statement of the various claimed embodiments.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

6.1 Claim 61 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

6.2 Claims 1-9, 33-35, 46, 48-50, 59-60, and 63-64 stand rejected under 35 U.S.C. § 103(a) as being obvious over Manning (U.S. 5,610,864; hereinafter "Manning") in view of Roy (U.S. 6,065,092; hereinafter "Roy") or Ogawa (U.S. 5,293,347; hereinafter "Ogawa").

In response to the Notice of Non-Compliant Appeal Brief mailed on July 12, 2007, it is respectfully noted that the double-patenting rejection of claims 59-60 is not appealed herein, and therefore, this subject matter is not addressed in this Amended Appeal Brief.

7. ARGUMENT

7.1 The Rejection under 35 U.S.C. § 112

Claim 61 was rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement. It has also been requested that certain claimed elements be added to the drawings. Because a *prima facie* case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as-filed, the Appellant respectfully traverses this rejection.

It is asserted in the Office Action that the limitation "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" was not described in the specification. However, merely asserting that a particular embodiment has been disclosed in FIG. 17, and noting that claim 61 does not cover that particular embodiment does not take into account the numerous other embodiments that have been described, both in the application text, and in the figures. In other words, FIG. 17 is not to be considered as effectively limiting all possible embodiments. Rather, this figure illustrates only some of many possible embodiments.

To demonstrate that the recited elements of claim 61 are indeed present in the Application, the Appellant has made numerous references in other responses to the following Application text: pg. 27, lines 1-11; pg. 38, lines 11-15; and pg. 39, lines 9-16. The attention of the reader is also directed to pg. 33, lines 13-21 and pg. 38, lines 11-15 of the Application. In these passages it is noted that some embodiments enable "using an initial externally generated address followed by one or more internally generated addresses" as well as "switching between burst access ... and ... pipelined modes of operation without ceasing." Finally, as noted on pg. 27, lines 5-11, "After a first /CAS signal 114 cycle in burst mode which uses the initial external values supplied for addresses XA0 and XA1, counter 149 increments those initial values and provides new internally generated addresses A0 and A1 by supplying count 0 signal 140 and count 1 signal 141 to respective A0 and A1 locations in temporary storage 119 through MUXs

125, 124. In this manner, internal addresses may be generated based on an initial external address."

Given the wide variety of described embodiments, it should be clear that if a pipelined mode is selected prior to entering the burst mode, with an external address supplied, and then the burst mode is selected thereafter, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" is indeed possible.

In addition, it is respectfully noted that "An application need not contain a word-for-word description of the claimed invention to satisfy the written description requirement. ... All that is needed is that the application reasonably convey the claimed subject matter." See Patent Prosecution: Practice and Procedure Before the U.S. Patent Office by Irah H. Donner, pg. 738, 2002. Given the written description, and the activity of the embodiments described with respect to selecting true pipelined and burst modes (which is not permitted by the cited art), the limitation "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation" has indeed been described in multiple ways as a part of the Application as-filed. This same reasoning applies to supporting the recited elements of "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation" and "providing a new external address for every access associated with accessing the asynchronously-accessible memory device while in the burst mode of operation."

To establish a *prima facie* case of lack of written description under § 112, each one of four elements must be demonstrated. Viz, (1) the application does not reasonably describe or convey the concepts (2) to one of ordinary skill in the art (3) at the time of filing the patent application (4) of the claimed invention. None of the elements has been shown. Therefore, since a *prima facie* case of lack of written description has not been made, and because the requisite information has indeed been disclosed in the Application as-filed, it is respectfully requested that the rejection under 35 USC § 112, first paragraph, be reconsidered and withdrawn.

7.2 The Rejection under 35 U.S.C. § 103

Claims 1-9, 33-35, 46, 48-50, 59-60 and 63-64 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Manning in view of Roy or Ogawa. First, the Appellant does not admit that Manning, Ogawa, or Roy are prior art, and reserves the right to swear behind these references in the future. Second, because no proper *prima facie* case of obviousness has been established, the Appellant respectfully traverses this rejection.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). The M.P.E.P. contains explicit direction to the Examiner in accordance with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck* , 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

No proper *prima facie* case of obviousness has been established because (1) combining the references does not teach all of the limitations set forth in the claims, (2) there is no motivation to combine the references, and (3) combining the references provides no reasonable expectation of success. Each of these points will be explained in detail, as follows.

The Combination of References Does not Teach All Limitations: As stated by the Board of Patent Appeals and interferences (BPAI), "Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's

suggestion to use a pipeline architecture is insufficient to suggest switching between burst and pipelined modes. As indicated supra, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection ...". BPAI, Appeal No. 2005-1725, March. 20, 2006. Thus, Manning fails to teach switching between burst and pipelined modes. This is also the case with Roy and Ogawa.

Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. *See* Roy, Col. 26, lines 62-66. New actions may be initiated when a burst is completed. *See Id.* at Col. 27, lines 4-14. The device may also be used in a pseudo-pipelined access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. *See Id.* at Col. 28, lines 16-32 and Col. 33, lines 8-19. While limited access pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. *See Id.* at Col. 33, lines 65-67. This is in direct contrast to the teachings of the Appellant, which enable true pipelined operation, with column-based switching in addition to row-based switching (See Application, pg. 38, lines 7-16). The Appellant was unable to find any indication that Roy enables selecting true pipelined and burst operation "on the fly" as demonstrated by the Appellant's disclosed embodiments (due to restriction imposed by software header mode changes and channel data/address sharing). For example, Roy does not permit row-based switching operation (i.e., "... cannot be used to change a row in every cycle ..."). *Id.* at Col. 38, lines 23-24.

While claims during examination should be interpreted as broadly as their terms reasonably allow, that interpretation must be tempered by the context in which the terms are used. The *Hyatt* court states that "during examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 U.S.P.Q.2D (BNA) 1664, 1667 (Fed. Cir. 2000) (emphasis added) ("During examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification."; citing *In re Graves*, 69 F.3d 1147, 1152, 36 U.S.P.Q.2D (BNA) 1697,

1701 (Fed. Cir. 1995); *In re Etter*, 756 F.2d 852, 858, 225 U.S.P.Q. (BNA) 1, 5 (Fed. Cir. 1985) (en banc).).

The interpretation of the term "pipelined mode" proffered by the Office with respect to Roy is neither reasonable, nor consistent with the specification. It is not reasonable because it distorts the meaning of the term as understood by those of skill in the art. The interpretation by the Office is also not consistent with the specification. Thus, any attempt by the Office to characterize Roy as teaching a true "pipelined mode" of operation is beyond that which should be reasonably allowed, and the rejection of claims using this reference under 35 U.S.C. § 103(a) is improper.

Ogawa presents similar difficulties, since pipelined access is described only with respect to a single mode of operation – the page mode. *See* Ogawa, Abstract and Col. 1, lines 8-12. "The page mode processing is an operation that subsequently reads out data in memory cells connected to one word line selected by a row address by sequentially changing the column address ...". Col. 4, lines 4-8. While Ogawa notes that "the present invention is not limited to the page mode, and the concept of the present invention can be similarly applied to random read/write operation" at Col. Col. 12, lines 5-10, this statement of potential use with respect to random read/write operations does not lead one of ordinary skill to understand how switching between burst and pipelined modes would be accomplished, since Ogawa does not teach any kind of switching behavior. As is the case with Roy, Ogawa provides no indication of how memory access operations can be conducted in conjunction with switching between burst an pipelined modes "on the fly" as taught by the Appellant.

Finally, as noted by the BPAI, "Manning's suggestion to use a pipelined structure is insufficient to suggest switching between burst and pipelined modes. As indicated supra, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur." BPAI, Appeal No. 2005-1725, March. 20, 2006. The Appellant also finds nothing in Manning to suggest substituting a pipelined mode for the page mode, as suggested by the Office with respect to Ogawa. Therefore, no combination of Manning and either Roy or Ogawa can provide "choosing whether the memory is in a burst mode of operation or a pipelined mode of operation" or "selecting a burst or

a pipeline mode of operation", much less "mode circuitry configured to select between a burst mode and a pipelined mode" as claimed by the Appellant.

No Motivation to Combine the References: The Office asserts that "it would have been obvious ... to modify the page mode of Manning to a pipeline mode of [Roy or] Ogawa because it would increase the memory throughput speed in Manning by providing a new column address every cycle." However, this suggestion to combine the references overlooks the fact that neither Manning nor Roy teach switching between a pipelined mode and another mode. Neither does Ogawa.

In addition, this assertion overlooks the limitations of Roy's pseudo-pipelined access, namely: (1) read operations are confined to the same row (no row-based switching), and (2) write operations only occur at one-half the channel speed; not at the full speed of the channel.

Finally, combining Roy with Manning ignores the following statement in Manning: "An integrated circuit memory device is designed for high speed data access and compatibility with *existing* memory systems." (Manning, Abstract, emphasis added). The device is made to be compatible with existing systems; not radically new systems, such as that described by Roy, in which "[o]ne of the fundamental features of this architecture is the use of the same lines of a data channel for both address and control information, as well as for bi-directional data transfers. Data read and write operations within the memory device are organized into discrete "transactions," with each such transaction initiated by several sequential data words termed a "header." The header includes address and control information for a subsequent transfer of one or more bytes of data into or out of the memory device. The header can be applied to one channel for a subsequent transaction across that same channel or across another channel." *Roy*, Col. 9, lines 12-22. Thus, Manning teaches away from the asserted combination, since the two devices are fundamentally incompatible. Therefore, since there is no evidence in the record to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is actually using personal knowledge, and the Examiner is again respectfully requested to submit an affidavit supporting such knowledge as required by 37 C.F.R. § 1.104(d)(2).

It is respectfully noted that the test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved

by the combination of elements that define the invention. *See Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985) (emphasis added). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02. Since Roy teaches away from using a true pipelined mode (as well as from being used in a conventional manner), and since Ogawa teaches away from any kind of mode switching during operation, there is no motivation to combine these references.

No Reasonable Expectation of Success: Roy teaches the use of a pseudo-pipelined mode. Ogawa teaches the use of a single mode of operation, without switching. Combining either of these references with Manning would not lead one of ordinary skill in the art to expect success, since the function of switching between burst and pipelined modes would not be enabled, nor would the design of circuitry configured to select between burst and pipelined modes of operation.

The use of unsupported assertions in the Office Action does not satisfy the explicit requirements needed to demonstrate motivation as set forth by the *In re Sang Su Lee* court. Therefore, the Examiner appears to be using personal knowledge, and is again respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). To-date, no such affidavit has been provided.

In summary, the references neither teach nor suggest selecting/choosing between burst and pipelined modes of operation, and the modifications suggested by the Office do not lead to a reasonable expectation of success by one of ordinary skill in the art. In fact, each of the references teach away from the suggested combination. Thus, the requirements of *M.P.E.P.* § 2142 have not been satisfied; and a *prima facie* case of obviousness has not been established with respect to the Appellant's claims. It is therefore respectfully requested that the rejection of claims 1-9, 33-35, 46, 48-50, 59-60 and 63-64 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

8. SUMMARY

For the reasons set forth above, no proper *prima facie* case of non-compliance with the written description requirement with respect to claim 61, nor of obviousness with respect to claims 1-9, 33-35, 46, 48-50, 59-60 and 63-64 has been properly established. Reversal of the rejections and allowance of the pending claims are therefore respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 13th day of August 2007.

Name Amy Moriarty

Signature

CLAIMS APPENDIX

1. An asynchronously-accessible storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode; and

circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.

2. The asynchronously-accessible storage device of Claim 1 wherein the burst mode and the pipelined mode are extended data out modes of operation.

3. The asynchronously-accessible storage device of Claim 1 wherein the pipelined mode is an extended data out mode.

4. The asynchronously-accessible storage device of Claim 1 wherein the burst mode is an extended data out mode.

5. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst mode circuitry includes a buffer, the buffer for storing an address.

6. The asynchronously-accessible storage device of Claim 5 wherein the pipelined/burst mode circuitry includes at least one counter for incrementing the address.

7. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst mode circuitry is coupled for reading an external address.

8. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes a buffer for storing the external address.

9. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes multiplexed devices for providing an internally generated address to the storage device.

33. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device;

selecting between outputting information from the storage device and inputting information to the storage device;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

34. The method of Claim 33, further comprising switching between the burst mode and the pipelined mode.

35. The method of Claim 33, wherein the second address is an external address.

46. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipelined mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined mode of operation;

switching modes to a burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation.

48. The method of Claim 46 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 46 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and

a system clock coupled to the microprocessor.

59. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

60. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between outputting information from the storage device and inputting information to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipeline mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation;

switching modes to a burst mode of operation;

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation; and providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation.

63. A storage device, comprising:

an array of memory cells;

mode circuitry for receiving a burst/pipeline signal; and

operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation.

64. A memory circuit, comprising:

an array of memory cells;

burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit; and

mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

Copies of the decisions in related appeals 2004-0414, 2004-1705, and 2005-1725 are attached.